

UIP E J037 33
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PATENT & TRADEMARK OFFICE

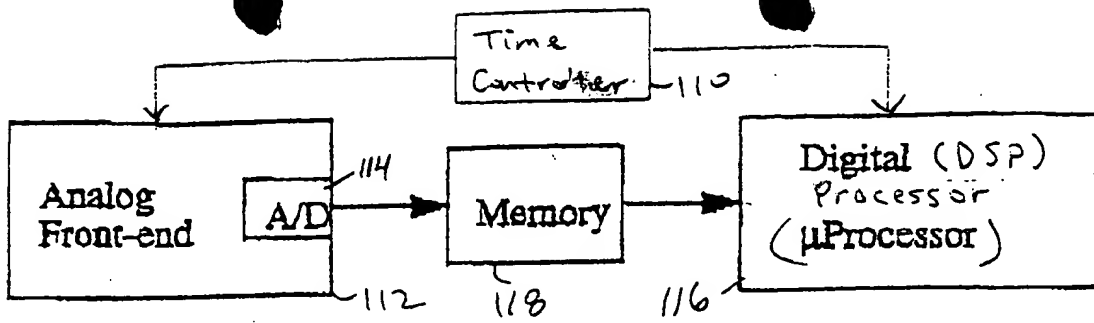


Figure 1: Receiver Block Diagram

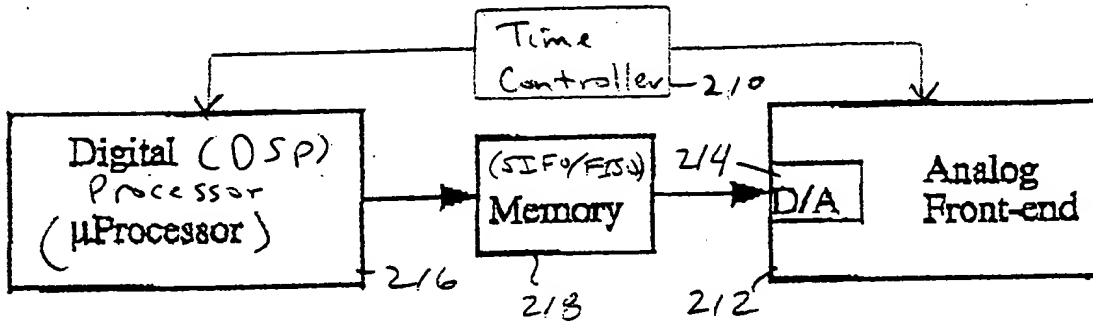


Figure 2: Transmitter Block Diagram

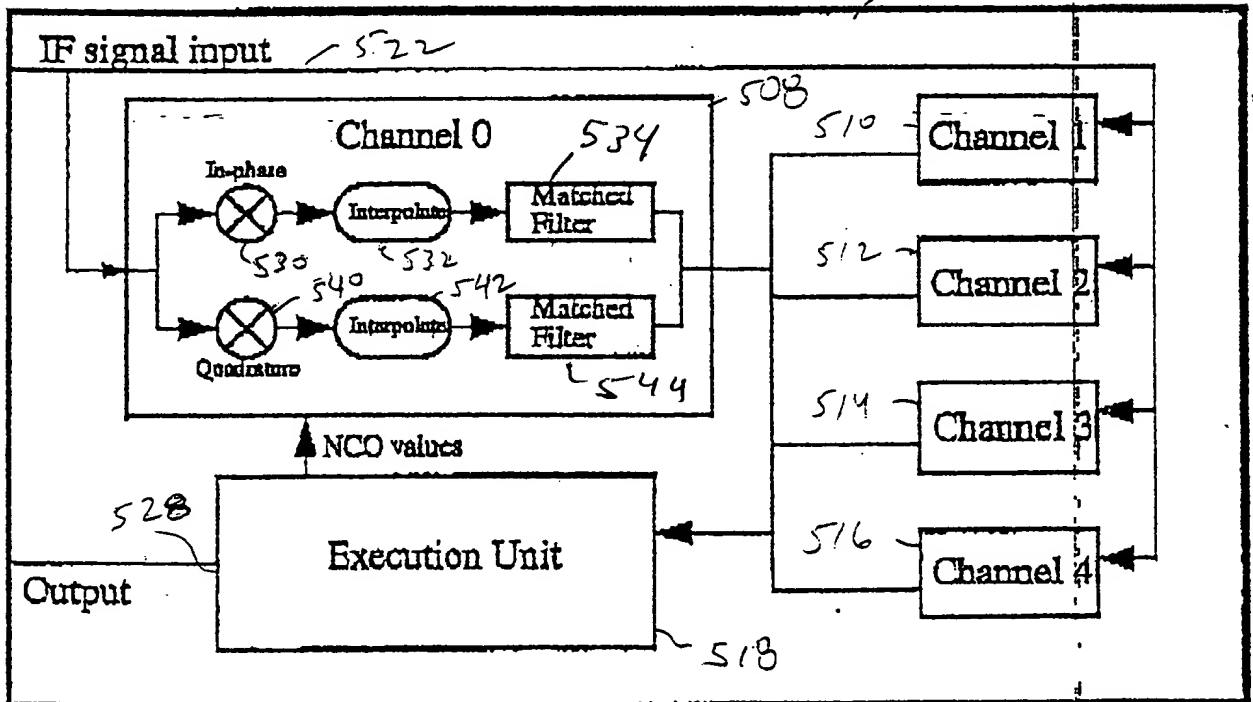


Figure 5 Synchronizer Architecture